REMARKS

Claims 1-5, 7-24, 26-28 and 30-42 are currently pending in the subject application and are presently under consideration. Claims 1, 2, 3, 7, 14, 20, 22, 28, 30 and 34 have been amended. Claims 6, 25 and 29 have been cancelled. New claim 43 has been added. Support for these amendments can be found in the specification especially at page 8 lines 6-7 and lines 23-26. A listing of claims can be found at pages 3-10 of the Reply. In addition, the Abstract and description have been amended as shown at page 2 of the Reply.

Favorable reconsideration of the subject patent application is respectfully requested in view of the comments and amendments herein.

I. Rejection of Claims 1-10 and 13 Under 35 U.S.C. §102(b)

Claims 1-10 and 13 stand rejected under 35 U.S.C. §102(b) as being anticipated by Lin *et al.* (U.S. 6,141,768). It is respectfully requested that this rejection be withdrawn for at least the following reasons. Lin *et al.* fails to teach or suggest each and every aspect of the subject claims.

> A single prior art reference anticipates a patent claim only if it ***expressly or inherently describes each and every limitation*** set forth in the patent claim. *Trintec Industries, Inc. v. Top-U.S.A. Corp.,* 295 F.3d 1292, 63 USPQ2d 1597 (Fed. Cir. 2002); *See Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). ***The identical invention must be shown in as complete detail as is contained in the ... claim***. *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The claimed subject matter relates to a RAM device, which can self-test and self-correct errors. The RAM device or card contains a memory array and an embedded self-testing RAM interface that contains a microprocessor that facilitates testing of the memory array. Such a modification adds intelligence and control to an otherwise passive memory array. Among other advantages, this leads to faster testing of the memory array wherein the CPU and the microprocessor divide the memory array, so that each of the CPU and the microprocessor can simultaneously test portions of the array. To this end independent claim 1 describes ***a self-testing RAM interface that includes a microprocessor, the self-testing RAM interface is embedded on a circuit board with the memory array,*** *the self-testing RAM interface tests integrity of data stored in the memory array; and* ***the self-testing RAM interface with the***

memory array and a central processing unit (CPU) of the computer are formed on separate integrated circuits. Lin *et al.* fails to disclose such novel aspects.

Lin *et al.* provides a computer system, which performs a self-test of the memory cells of a memory device prior to loading of a computer program into the memory device, so as to determine the locations of defective memory cells. The CPU of the computer system carries out this testing of memory cells (See for e.g. col. 5 lines 12-16 of Lin *et al.*) On page 3 of the Office Action it is incorrectly contended that Lin et al. teaches a RAM device including a microprocessor at col. 6 lines 30-33. At the cited section, an 80X86 microprocessor is employed as an example whose machine code of "EB0800" stands for a "JUMP" step that skips 8 bytes of data after the "JUMP" instruction. None of the details of the RAM device employed by Lin et al. at col. 4 lines 14-18 and Fig. 2b reveal ***a self-testing RAM interface that includes a microprocessor, the self-testing RAM interface is embedded on a circuit board with the memory array.*** In view of at least the above it is clear that an invention identical to that recited in the subject claims is neither taught nor suggested by the cited document. Hence withdrawal of this rejection is respectfully requested with respect to independent claim 1 and all the claims that depend there from.

II. Rejection of Claims 14, 15, 17, 34, 35 and 42 Under 35 U.S.C. §102(e)

Claims 14, 15, 17, 34, 35 and 42 stand rejected under 35 U.S.C. §102(e) as being anticipated by Olarig (U.S. 6,505,305). It is respectfully requested that this rejection be withdrawn for at least the following reasons. Olarig fails to teach or suggest each and every aspect of the subject claims.

The claimed invention relates to a system and method for self-testing and correcting memory devices comprising a processor to carry out the testing procedures. Such an intelligent memory device mitigates the need for a central processor unit in a computer system to be diverted from other processes to test and correct the memory device. To this end independent claims 14 recites ***a second microprocessor embedded in a single circuit board with the memory banks, the CPU and the memory banks are embedded in separate circuit boards*** or similarly claim 34 recites ***the self-testing RAM interface further comprises a microprocessor, and the interface is part of a circuit board that includes the memory location.*** Olarig teaches a fail-over feature for handling of memory access errors in a computer system. Generally the fail over

system described is part of the CPU section and is part of or connected to a memory controller (See for e.g. Olarig col. 5 lines 38-40). In contrast Applicant's claimed invention discloses ***a second microprocessor embedded in a single circuit board with the memory banks, the CPU and the memory banks are embedded in separate circuit boards.*** Nowhere does Olarig teach or suggest such novel aspects. By including a microprocessor along with the RAM device the claimed invention mitigates the need for such fail-over features to be included with the CPU as taught by Olarig. Therefore it is clear that the cited reference neither teaches nor suggests the invention as recited in the independent claims 14 and 34. In view of at least the above withdrawal of this rejection is requested with respect to independent claims 14, 34 and all the claims that depend there from.

III. Rejection of Claims 14, 17, 34, 35 and 42 Under 35 U.S.C. §102(e)

Claims 14, 17, 34, 35 and 42 stand rejected under 35 U.S.C. §102(e) as being anticipated by Callaway *et al.* (U.S. 6,879,530). It is respectfully requested that this rejection be withdrawn for at least the following reasons. Callaway *et al.* fails to teach or suggest each and every aspect of the subject claims.

The claimed invention relates to a system and method for self-testing and correcting memory devices comprising a separate processor for the memory array to carry out the testing procedures. Such an intelligent and self-testing RAM interface can effectuate all testing procedures to make portions of tested RAM available to the CPU while the CPU concurrently runs boot process therefore speeding up machine start up. To this end independent claim 14 recites ***a second microprocessor embedded in a single circuit board with the memory banks, the CPU and the memory banks are embedded in separate circuit boards*** or similarly claim 34 recites ***the self-testing RAM interface further comprises a microprocessor, and the interface is part of an integrated circuit that includes the memory location.*** Callaway *et al.* fails to teach or suggest such novel aspects. Callaway *et al.* relates to dynamically detecting and repairing faults in semiconductor memories by comparing multiple memory blocks against each other and then remapping failed memory blocks with unassigned spare memory blocks. However nowhere does Callaway *et al.* teach or suggest ***a second microprocessor embedded in a single circuit board with the memory banks, the CPU and the memory banks are embedded in separate circuit***

boards. None of the embodiments of memory devices disclosed by Callaway *et al.* include a microprocessor located on the same circuit board as the memory banks in a RAM device. In view of at least the aforementioned it is respectfully requested that this rejection be withdrawn with respect to independent claims 14, 34 and all the claims that depend there from.

IV. Rejection of Claims 22, 23 and 25-27 Under 35 U.S.C. §102(b)

Claims 22, 23 and 25-27 stand rejected under 35 U.S.C. §102(b) as being anticipated by Hayes *et al.* (U.S. 5,781,721). It is respectfully requested that this rejection be withdrawn for at least the following reasons. Hayes *et al.* fails to teach or suggest each and every aspect of the subject claims.

The subject invention relates to a system and method for testing, correcting and compensating for errors that do not significantly delay machine start up and which can continuously test for and correct errors while the system is operating. To this end independent claim 22 describes a method whereby a memory device tests itself. The memory device includes ***the self-testing RAM interface further comprising a microprocessor; the self-testing RAM interface is embedded with the memory cells on a single circuit board.*** Hayes *et al.* does not teach or suggest such novel aspects. Hayes *et al.* relates to a method and apparatus that permits testing of cache RAM on a microprocessor using static RAM test processes (See Hayes *et al.* col. 1 lines 19-21). Accordingly Hayes *et al.* teaches a microprocessor with on-board data cache and on-board instruction cache. Nowhere does Hayes *et al.* teach or suggest ***self-testing RAM interface further comprising a microprocessor; the self-testing RAM interface is embedded with the memory cells on a single circuit board*** as recited in independent claim 22. Hence an invention identical to that disclosed in the subject claims is not taught or suggested by Hayes *et al.* Therefore withdrawal of this rejection is respectfully requested.

V. Rejection of Claims 28-29 Under 35 U.S.C. §102(b)

Claims 28-29 stand rejected under 35 U.S.C. §102(b) as being anticipated by Crouch *et al.* (U.S. 5,617,531). The statute of 102 was not stated in the subject Office Action. According to the filing dates of the subject application and the cited document it is assumed that the Examiner meant a 102(b) rejection. Withdrawal of this rejection is respectfully requested for at

least the following reasons. Claim 29 has been cancelled. Crouch et al. neither teaches nor suggests an invention identical to that recited in the amended claim 28.

Crouch et al. teaches a method for internally testing a plurality of embedded memories of a data processor. The data processor has an internal test controller that generates a test pattern for each embedded memory within the plurality of embedded memories. In contrast, the subject invention relates to a self-testing RAM interface. Accordingly claim 28 recites ***a second microprocessor embedded in a single integrated circuit as the memory device, the CPU and the memory device are formed of different integrated circuits.*** The second processor included with the self-testing RAM interface adds intelligence and control to an otherwise passive RAM device. This significantly impacts the system performance in part because the CPU of a computer need not be diverted from other tasks to test and correct a memory device. Therefore it is clear that an identical invention as disclosed in claim 28 is not taught or suggested by Crouch *et al.* Accordingly withdrawal of this rejection is respectfully requested.

VI. Rejection of Claim 11 Under 35 U.S.C. §103(a)

Claim 11 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Lin *et al.* in view of Microsoft Computer Dictionary (fifth edition). It is submitted that this rejection be withdrawn for at least the following reasons. Neither Lin *et al.* nor Microsoft Computer Dictionary alone or in combination, teach or suggest an invention as recited in the subject claims.

Claim 11 depends from independent claim 1 and, as stated *supra*, Lin *et al.* does not teach or suggest all limitations of claim 1 and Microsoft Computer Dictionary fails to make up for the aforementioned deficiencies. In particular the cited documents either alone or in combination do not teach or suggest ***a self-testing RAM interface that includes a microprocessor, the self-testing RAM interface is embedded on a circuit board with the memory array,*** *the self-testing RAM interface tests integrity of data stored in the memory array; and* ***the self-testing RAM interface with the memory array and a central processing unit (CPU) of the computer are formed on separate integrated circuits*** as recited in independent claim 1. Hence it follows that dependent claim 11 which adds further details to independent claim 1 would be non-obvious over a combination of the cited documents. Therefore withdrawal of this rejection is requested.

VII. Rejection of Claim 12 Under 35 U.S.C. §103(a)

Claim 12 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Lin in view of Wyatt *et al.* (U.S. 6,968,479). It is submitted that this rejection be withdrawn for at least the following reasons. Neither Lin *et al.* nor Wyatt *et al.* alone or in combination, teach or suggest an invention as recited in the subject claims.

Claim 12 depends from independent claim 1 and, as stated *supra*, Lin *et al.* does not teach or suggest all limitations of claim 1 and Wyatt *et al.* fails to make up for the aforementioned deficiencies. In particular the cited documents either alone or in combination do not teach or suggest ***a self-testing RAM interface that includes a microprocessor, the self-testing RAM interface is embedded on a circuit board with the memory array,*** *the self-testing RAM interface tests integrity of data stored in the memory array; and* ***the self-testing RAM interface with the memory array and a central processing unit (CPU) of the computer are formed on separate integrated circuits*** as recited in independent claim 1. Therefore it follows that dependent claim 12 which adds further details to independent claim 1 would be non-obvious over a combination of the cited documents. Therefore withdrawal of this rejection is requested.

VIII. Rejection of Claim 16 Under 35 U.S.C. §103(a)

Claim 16 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Olarig in view of Microsoft Computer Dictionary (fifth edition). This rejection should be withdrawn for at least the following reasons. The cited references, either alone or in combination, fail to teach or suggest all aspects of the subject claims.

Claim 16 depends directly from independent claim 14. As discussed *supra* in connection with independent claim 14, Olarig does not teach or suggest ***a second microprocessor embedded in a single circuit board as the memory banks, the CPU and the memory banks are embedded in separate circuit boards*** and Microsoft Computer Dictionary fails to make up for this deficiency. At the cited section, Microsoft Computer Dictionary does not teach or suggest ***a second microprocessor embedded in a single circuit board as the memory banks, the CPU and the memory banks are embedded in separate circuit boards.*** Therefore this rejection of claim 16 should be withdrawn.

IX. Rejection of Claims 18 and 19 Under 35 U.S.C. §103(a)

Claims 18 and 19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Olarig in view of Callaway *et al.* This rejection should be withdrawn for at least the following reasons. The cited references, either alone or in combination, fail to teach or suggest all aspects of the subject claims. Claim 18 depends directly from independent claim 14 while claim 19 depends on claim 18. As discussed *supra* in connection with independent claim 14, neither Olarig nor Callaway *et al.* teach or suggest ***a second microprocessor embedded in a single circuit board as the memory banks, the CPU and the memory banks are embedded in separate circuit boards***. Therefore this rejection should be withdrawn.

X. Rejection of Claim 21 Under 35 U.S.C. §103(a)

Claim 21 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Callaway *et al.* in view of Microsoft Computer Dictionary (fifth edition). This rejection should be withdrawn for at least the following reasons. The cited references, either alone or in combination, fail to teach or suggest all aspects of the subject claims.

Claim 21 depends directly from independent claim 20. Claim 20 recites ***a microprocessor embedded with the memory stores on a circuit board; a self-testing interface that includes the microprocessor and*** *maps input addresses and data to a multitude of memory cells on a plurality of memory stores to facilitate accurate data storage and retrieval, wherein the memory cells store copies of the input data.* Callaway *et al.* fails to teach or suggest such novel aspects. Callaway *et al.* relates to a dynamic random access memory, which includes circuitry for dynamically storing memory element remapping information. However nowhere does Callaway *et al.* teach or suggest a self-testing interface, which integrates a microprocessor with memory stores. This provides an intelligent memory system that significantly reduces start up time by mitigating the need for a central processing unit to be diverted from other tasks in order to initiate testing procedures. Therefore it is requested that this rejection be withdrawn.

XI. Rejection of Claim 24 Under 35 U.S.C. §103(a)

Claim 24 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Hayes *et al.* in view of Microsoft Computer Dictionary (fifth edition). This rejection should be withdrawn for

at least the following reasons. The cited documents, either alone or in combination, fail to teach or suggest all aspects of the subject claims.

Claim 24 depends directly from independent claim 22. As discussed *supra* in connection with independent claim 22, Hayes *et al.* does not teach or suggest ***the self-testing RAM interface further comprising a microprocessor, the self-testing RAM interface is embedded with the memory cells on a single integrated circuit*** and Microsoft Computer Dictionary fails to make up for this deficiency. At the cited section, Microsoft Computer Dictionary does not teach or suggest ***self-testing RAM interface comprising a microprocessor, which is embedded along with the memory cells.*** Therefore this rejection of claim 24 should be withdrawn.

XII. Rejection of Claims 30-33, 36, 37 and 41 Under 35 U.S.C. §103(a)

Claims 30-33, 36, 37 and 41 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Olarig in view of Hayes *et al.* This rejection should be withdrawn for at least the following reasons. The cited documents, either alone or in combination, fail to teach or suggest all aspects of the subject claims.

The subject invention relates to a RAM device, which can self-test and self-correct errors. The RAM device or card contains a memory array and an embedded self-testing RAM interface that contains a microprocessor that facilitates testing of the memory array. To this end independent claims 30 and 34 recite similar features namely***: the self-testing RAM interface further comprises a microprocessor, and the interface is part of an integrated circuit that includes the memory location.*** Hayes et al. relates to a method of testing cache memory on-board a microprocessor using standard SRAM testing algorithms and equipment. Olarig relates to a fail-over feature for handling of memory access errors in a computer system. However neither of the cited documents alone or in combination with each other teaches nor suggests a ***self-testing RAM interface further comprises a microprocessor, and the interface is part of an integrated circuit that includes the memory location*** as recited in independent claims 30 and 34. Therefore it is respectfully requested that this rejection be withdrawn with respect to independent claim 30, 34 and all the claims that depend there from.

XIII. New Claim 43

Newly added claim 43 emphasizes novel aspects of the invention discussed *supra* in connection with claims 1-5, 7-24, 26-28, and 30-42. Accordingly, this claim is patentably distinct over the art of record for at least the same reasons as are claims 1-5, 7-24, 26-28, and 30-42. Support for this claim can be found in the description at page 3 lines 24-26.

CONCLUSION

The present application is believed to be in condition for allowance in view of the above comments and amendments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [ALBRP324US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

AMIN, TUROCY & CALVIN, LLP

/Himanshu S. Amin/
Himanshu S. Amin
Reg. No. 40,894

AMIN, TUROCY & CALVIN, LLP
24TH Floor, National City Center
1900 E. 9TH Street
Cleveland, Ohio 44114
Telephone (216) 696-8730
Facsimile (216) 696-8731